

# AD7714YRUZ

Data Sheet

CMOS,  $3V\!/\!5V\!,\,500~\mu\text{A},\,24\text{-Bit}$  Sigma-Delta, Signal Conditioning ADC; Temperature Range: Industrial

Manufacturers	Analog Devices, Inc	
Package/Case	TSSOP-24	555555555 C
Product Type	Data Conversion ICs	
RoHS	Pb-free Halide free	
Lifecycle		Images are for reference only
Please submit REO for AD7714VRUZ or Email to us; sales@ovaga.com We will contact you in 12 hours REO		

# **General Description**

The part features three differential analog inputs (which can also be configured as five pseudo-differential analog inputs) as well as a differential reference input. The AD7714 thus performs all signal conditioning and conversion for a system consisting of up to five channels. A new Y grade has recently been added to the existing range. Compared to the A grades this new grade has an extended operating temperature range, schmitt trigger inputs on SCLK and DIN, tighter linearity specifications, lower power consumption and is available in a smaller package.

The AD7714 is ideal for use in smart microcontroller- or DSP-based systems. It features a serial interface that can be configured for three-wire operation. Gain settings, signal polarity and channel selection can be configured in software using the serial port. The AD7714 provides self-calibration, system calibration and background calibration options and also allows the user to read and write the on-chip calibration registers.

CMOS construction ensures very low power dissipation, and the power-down mode reduces the standby power consumption to 15  $\mu$ W typical at 3 V. Minimum operating voltage for the A grades is 3 V and 2.7 V for the Y grades. The A grades are available in a 24-pin, 0.3 inch-wide, plastic dual-in-line package (DIP); a 24 lead small outline (SOIC) package and a 28-lead shrink small outline package (SSOP). The new Y grade is available in a 24-pin, 0.3 inch-wide, plastic dual-in-line package (DIP); a 24 lead small outline package (SSOP). The new Y grade is available in a 24-pin, 0.3 inch-wide, plastic dual-in-line package (DIP); a 24 lead small outline (SOIC) package and a 24-lead Thin Shrink Small Outline Package (TSSOP).

## Features

Charge Balancing ADC24 Bits No Missing Codes0.0015% Nonlinearity

Five-Channel Programmable Gain Front EndGains from 1 to 128Can Be Configured as Three Fully DifferentialInputs or Five Pseudo-Differential Inputs

Three-Wire Serial InterfaceSPI®, QSPITM, MICROWIRETM and DSP Compatible

3 V (AD7714-3) or 5 V (AD7714-5) Operation

Low Current (350 µA typ) with Power-Down (5 µA typ)

Low Noise (<150 nV rms)

Low-Pass Filter with Programmable Filter Cutoffs

Please see data sheet for additional features

#### **Related Products**



ADAS3022BCPZ Analog Devices, Inc

LFCSP-40



Analog Devices, Inc PDIP-28

AD574AJNZ





LFCSP-32



AD7124-8BCPZ-RL7 Analog Devices, Inc



### AD7266BSUZ

Analog Devices, Inc TQPF-32



Analog Devices, Inc SOIC-16

**AD7401YRWZ** 

## AD7192BRUZ-REEL

Analog Devices, Inc TSSOP-24



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AD9680BCPZ-500

Analog Devices, Inc LFCSP-64

