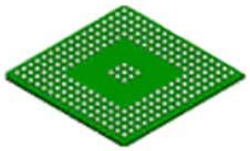
ADRV9009BBCZ

Data Sheet

RF Transceiver 1.3V/1.8V/1.89V 196-Pin CSP-BGA Tray

Manufacturers	Analog Devices, Inc
Package/Case	196-LFBGA, CSPBGA
Product Type	RF Integrated Circuits
RoHS	Pb-free Halide free
Lifecycle	



Images are for reference only

Please submit RFQ for ADRV9009BBCZ or Email to us: sales@ovaga.com We will contact you in 12 hours. RFQ

General Description

The ADRV9009 is a highly integrated, radio frequency (RF), agile transceiver offering dual transmitters and receivers, integrated synthesizers, and digital signal processing functions. The IC delivers a versatile combination of high performance and low power consumption demanded by 3G, 4G, and 5G macro cell time division duplex (TDD) base station applications.

The receive path consists of two independent, wide bandwidth, direct conversion receivers with state-of-the-art dynamic range. The device also supports a wide bandwidth, time shared observation path receiver (ORx) for use in TDD applications. The complete receive subsystem includes automatic and manual attenuation control, dc offset correction, quadrature error correction (QEC), and digital filtering, thus eliminating the need for these functions in the digital baseband. Several auxiliary functions, such as analog-to-digital converters (ADCs), digital-to-analog converters (DACs), and general-purpose inputs/outputs (GPIOs) for the power amplifier (PA), and RF front-end control are also integrated.

In addition to automatic gain control (AGC), the ADRV9009 also features flexible external gain control modes, allowing significant flexibility in setting system level gain dynamically.

The received signals are digitized with a set of four high dynamic range, continuous time Σ-Δ ADCs that provide inherent antialiasing. The combination of the direct conversion architecture, which does not suffer from out of band image mixing, and the lack of aliasing, relaxes the requirements of the RF filters when compared to traditional intermediate frequency (IF) receivers.

The transmitters use an innovative direct conversion modulator that achieves high modulation accuracy with exceptionally low noise.

The observation receiver path consists of a wide bandwidth, direct conversion receiver with state-of-the-art dynamic range.

The fully integrated phase-locked loop (PLL) provides high performance, low power, fractional-N RF frequency synthesis for the transmitter (Tx) and receiver (Rx) signal paths. An additional synthesizer generates the clocks needed for the converters, digital circuits, and the serial interface. A multichip synchronization mechanism synchronizes the phase of the RF local oscillator (LO) and baseband clocks between multiple ADRV9009 chips. Precautions are taken to provide the isolation required in high performance base station applications. All voltage controlled oscillators (VCOs) and loop filter components are integrated.

The high speed JESD204B interface supports up to 12.288 Gbps lane rates, resulting in two lanes per transmitter and a single lane per receiver in the widest bandwidth mode. The interface also supports interleaved mode for lower bandwidths, thus reducing the total number of high speed data interface lanes to one. Both fixed and floating point data formats are supported. The floating point format allows internal AGC to be invisible to the demodulator device.

The core of the ADRV9009 can be powered directly from 1.3 V regulators and 1.8 V regulators, and is controlled via a standard 4-wire serial port. Comprehensive power-down modes are included to minimize power consumption in normal use. The ADRV9009 is packaged in a 12 mm × 12 mm, 196-ball chip scale ball grid array (CSP_BGA).

Features

Dual transmitters

Dual receivers

Dual input shared observation receiver

Maximum receiver bandwidth: 200 MHz

Maximum tunable transmitter synthesis bandwidth: 450 MHz

Maximum observation receiver bandwidth: 450 MHz

Fully integrated fractional-N RF synthesizers

Fully integrated clock synthesizer

Multichip phase synchronization for RF LO and baseband clocks

JESD204B datapath interface

Tuning range (center frequency): 75 MHz to 6000 MHz

Application

3G, 4G, and 5G TDD macrocell base stations

TDD active antenna systems

Massive multiple input, multiple output (MIMO)

Phased array radar

Electronic warfare

Military communications

Portable test equipment

Related Products

ADL5330ACPZ

Analog Devices, Inc

LFCSP24

ADL5240ACPZ-R7

Analog Devices, Inc

LFCSP-32

AD630SD

Analog Devices, Inc

20 ld Side-BrazedCerDIP

ADRF5040BCPZ

Analog Devices, Inc

HIGH ISOLATION, SP4T, 9KHZ - 12G

AD607ARSZ-REEL

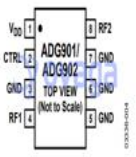
Analog Devices, Inc

SSOP-20

AD831AP

Analog Devices, Inc

20 ld PLCC



ADG901BRM

Analog Devices, Inc

MSOP-8

ADL5350ACPZ

Analog Devices, Inc

LFCSP-8