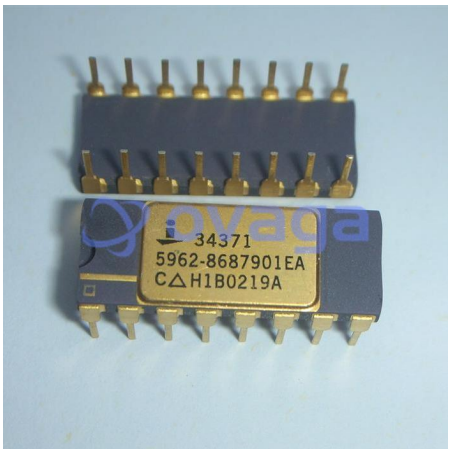
5962-8687901EA

Data Sheet

SMD VERSION HS1-3182 HT SUSA CODE:8542390000

Manufacturers	Renesas Technology Corp
Package/Case	CDIP-16
Product Type	Interface ICs
RoHS	
Lifecycle	



Images are for reference only

Please submit RFQ for 5962-8687901EA or Email to us: sales@ovaga.com We will contact you in 12 hours. RFQ

General Description

The HS-3182 is a monolithic dielectrically isolated bipolar differential line driver designed to meet the specifications of ARINC 429. This Device is intended to be used with a companion chip, HS-3282 CMOS ARINC Bus Interface Circuit, which provides the data formatting and processor interface function. All logic inputs are TTL and CMOS compatible. In addition to the DATA (A) and DATA (B) inputs, there are also inputs for CLOCK and SYNC signals which are AND'd with the DATA inputs. This feature enhances system performance and allows the HS-3182 to be used with devices other than the HS-3182. Three power supplies are necessary to operate the HS-3182: + = -15V ±10%, and = ±2VREF. Typically, = 5V ±5%, but a separate power supply may be used for VREF which should not exceed 6V. The driver output impedance is 75Ω ±20% at +25°C. Driver output rise and fall times are independently programmed through the use of two external capacitors connected to the CA and CB inputs. Typical capacitor values are = 75pF for high-speed operation (100kBPS), and = 300pF for low-speed operation (12kBPS to 14.5kBPS). The outputs are protected against overvoltage and short circuit as shown in the Block Diagram. The HS-3182 is designed to operate over an ambient temperature range of -55°C to +125°C, or -40°C to +85°C.

Features

RoHS/Pb-free Available for SBDIP Package (100% Gold Termination Finish)

TTL and CMOS Compatible Inputs

Adjustable Rise and Fall Times via Two External Capacitors

Programmable Output Differential Voltage via V_{REF} Input

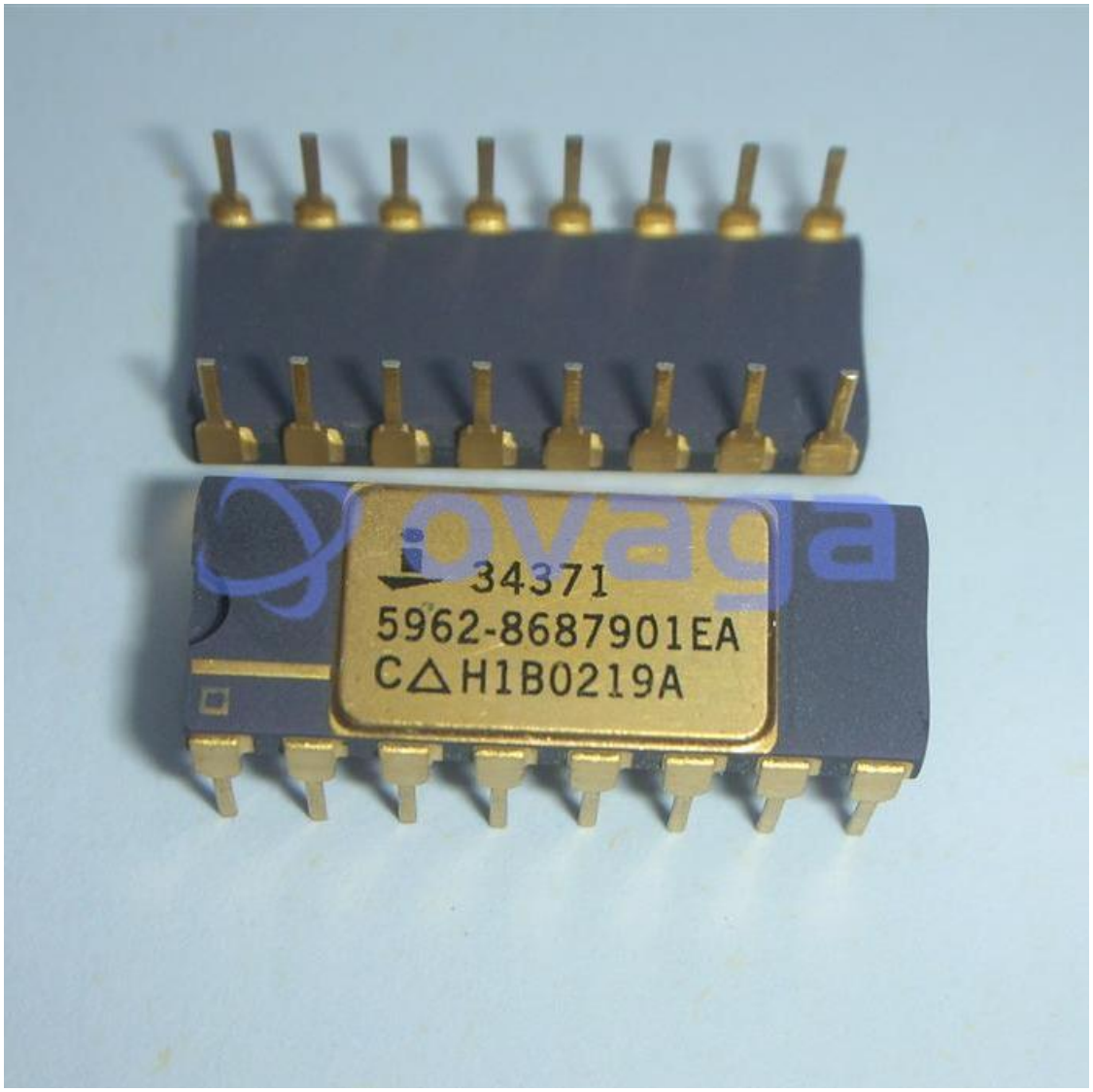
Operates at Data Rates Up to 100k Bits/s

Output Short Circuit Proof and Contains Overvoltage Protection

Outputs are Inhibited (0V) If DATA (A) and DATA (B) Inputs are Both in the "Logic One" State

DATA (A) and DATA (B) Signals are "AND'd" with Clock and Sync Signals

Full Military Temperature Range

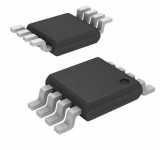


Related Products

[5962-9052501MQA]

Renesas Technology Corp

CDIP40



[ISL3259EIUZ]

Renesas Technology Corp

MSOP-8

[ISL54059IRTZ]

Renesas Technology Corp

DFN3x3-10

[ISL3259EIBZ]

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SOP-8

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[5962-9052502MQA]

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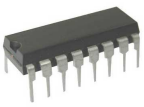
CDIP40



[5962-9204201MEA]

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DIP-16

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