IC ETHERNET SWITCH 7PORT 128TQFP

Manufacturers	Microchip Technology, Inc
Package/Case	TQFP-128
Product Type	Integrated Circuits (ICs)
RoHS	
Lifecycle	

Images are for reference only

Please submit RFQ for KSZ9477STXI-TR or Email to us: sales@ovaga.com We will contact you in 12 hours.　　　RFQ

General Description

The KSZ9477 is a fully integrated layer 2, managed,seven-port gigabit Ethernet switch with numerousadvanced features. Five of the seven ports incorporate10/100/1000 Mbps PHYs. The other two ports haveinterfaces that can be configured as SGMII, RGMII, MII or RMII.Either of these may connect directly to a host processor orto an external PHY. The SGMII port may interface to a fiber optic transceiver.

Full register access is available by SPI or I2C interfaces,and by optional in-band management via any of the data ports.PHY register access is provided by a MIIM interface.

Security features include support for IEEE 802.1X port-based authentication and Access Control List (ACL) filtering.

As a member of the EtherSynch® product family, theKSZ9477 incorporates full hardware support for the IEEE1588v2 Precision Time Protocol (PTP), including hardwaretime-stamping at all PHY-MAC interfaces, and a high-resolution hardware "PTP clock". IEEE 1588 provides sub-microsecond synchronization for a range of industrialEthernet applications.

The KSZ9477supports time-stamping and time-keeping featuressupport IEEE 802.1AS time synchronization. All portsfeature credit based traffic shapers for IEEE 802.1Qav,and a time aware scheduler as proposed for IEEE802.1Qbv.

The KSZ9477 also incorporates features that simplify theimplementation of DLR and HSR redundancy protocols byoff-loading tasks from the host processor. For DLRnetworks, these features include Beacon framegeneration, Beacon timeout detection, and MAC tableflushing. HSR networks are supported with automaticduplicate frame discard, and self-address filtering.

An assortment of power-management features includingEnergy-Efficient Ethernet (EEE) have been designed in tosatisfy energy efficient environments.

Looking for a Linux® Host Processor, try the SAMA5D3.

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Features

Integrated 7-port 10/100/1000 Layer-2 switch with Gigabit uplink

Non-blocking wire-speed Ethernet switching fabric

IEEE802.1Qav (AVB) credit based traffic shaper

Time aware traffic scheduler with low latency cut- through mode

IEEE1588v2 Precision Time Protocol support

Time-stamping on all ports

Precision GPIO pin timed to the AVB/1588 clock

DLR (EtherNet/IP) support

HSR (IEC 62439-3) support

Full-featured forwarding and filtering control, including Access Control List (ACL) filtering

IEEE802.1X support (Port-Based Network Access Control)

IEEE802.1Q VLAN support for 128 active VLAN groups and the full range of 4096 VLAN IDs

IEEE802.1p/Q tag insertion or removal on a per port basis and support for double-tagging

VLAN ID tag/untag options on per port basis

IEEE802.3x full-duplex flow control and half-duplex back pressure collision control

IGMPv1/v2/v3 snooping for multicast packet filtering

IPv6 multicast listener discovery (MLD) snooping

QoS/CoS packets prioritization support: 802.1p, DiffServ-based and re-mapping of 802.1p priority field per-port basis on four priority levels

IPv4/IPv6 QoS support

Programmable rate limiting at ingress and egress ports

Broadcast storm protection

Four priority queues with dynamic packet mapping for IEEE802.1p, IPv4 DIFFSERV, IPv6 TrafficClass

MAC filtering function to filter or forward unknown unicast, multicast and VLAN packets

Self-address filtering for implementing ring topologies

Comprehensive Configuration Register Access

High-speed SPI (4-wire, up to 50MHz) interface to access all internal registers

I2C Interface to access all registers

MII management (MIIM, MDC/MDIO 2 wire) interface to access all PHY registers per IEEE 802.3 specification

In-band management to access all registers via any of the seven ports, strap enabled

I/O pin strapping facility to set certain register bits from I/O pins at reset time

Control registers configurable on-the-fly

Switch Monitoring Features

Port mirroring/monitoring/sniffing: ingress and/or egress traffic to any port or MII/RMII

MIB counters for fully-compliant statistics gathering (34 MIB counters per port)

Low Power Dissipation

Full-chip software power-down

Energy detect power-down (EDPD)

Wake on LAN (WoL) support

Related Products

KSZ9563RNXI

Microchip Technology, Inc

VQFN-64

KSZ8001L

Microchip Technology, Inc

LQFP-48

KSZ9896CTXI-TR

Microchip Technology, Inc

TQFP-128

KSZ9563RNXC

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LQFP-80