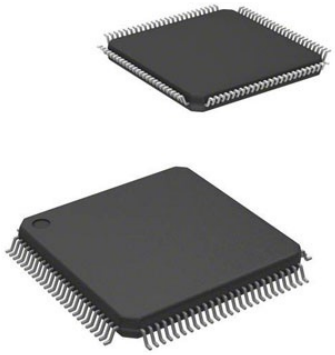
ATSAM4SD32CA-AU

Data Sheet

ARM MCU, SAM4S Series, SAM32 Family SAM 4S Series Microcontrollers, ARM Cortex-M4, 32bit, 120 MHz

Manufacturers	Microchip Technology, Inc
Package/Case	LQFP-100
Product Type	Embedded Processors & Controllers
RoHS	Green
Lifecycle	



Images are for reference only

Please submit RFQ for ATSAM4SD32CA-AU or Email to us: sales@ovaga.com We will contact you in 12 hours. RFQ

General Description

For New Designs, we highly recommend to consider Revision B for Prototypes and Production.

Microchip'sARM-based SAM4SD32 microcontroller builds on the high-performance 32-bit Cortex®-M4 core.

The SAM4SD32 features:

2MB of flash memory and 160KB of SRAM

2KB of integrated cache memory

Maximum operating speed of 120MHz

Dual-bank Flash

Best-in-class power consumption: 200uA/MHz in active mode, down to 1uA at 1.8V in back-up mode with the RTC running

1.62V to 3.6V power supply

Extensive peripheral set for connectivity, system control and analog interfacing

Pin-to-pin compatible with Microchip SAM7S, SAM3N and SAM3S MCUs

Supported by Atmel Studio, Software Framework(ASF) and the SAM4S-EK2

Features

ARM Cortex-M4 with 2 Kbytes Cache running at up to 120 MHz

Memory Protection Unit (MPU)

DSP Instructions, Thumb®-2 instruction set

2 x 1024 Kbytes Dual-Bank embedded Flash, ECC, Security Bit and Lock Bits

60 Kbytes embedded SRAM

16 Kbytes ROM with embedded boot loader routines (UART, USB) and IAP routines

8-bit Static Memory Controller (SMC): SRAM, PSRAM, NOR and NAND Flash support

External Bus Interface - 8-bit data, 4 chip selects, 24-bit address

Embedded voltage regulator for single-supply operation

Power-on-Reset (POR), Brown-out Detector (BOD) and Dual Watchdog for Safe Operation

Quartz or ceramic resonator oscillators: 3 to 20 MHz with clock failure detection and 32.768 kHz for RTT or system clock

RTC with Gregorian and Persian Calendar Mode, Waveform Generation in Backup mode

RTC counter calibration circuitry compensates for 32.768 kHz crystal frequency inaccuracy

Slow clock internal RC oscillator as permanent low-power mode device clock

High-precision 8/12 MHz factory-trimmed internal RC oscillator with 4 MHz default frequency for device startup, in-application trimming access for frequency adjustment

Two PLL up to 240 MHz for Device Clock and for USB

Temperature Sensor

Low-power tamper detection on two inputs, anti-tampering by immediate clear of general-purpose backup registers (GPBR)

22 Peripheral DMA Controllers

Sleep, Wait and Backup modes; consumption down to 1 µA in Backup mode

100-lead LQFP, 14 x 14 mm, pitch 0.5 mm

100-lead TFBGA, 9 x 9 mm, pitch 0.8 mm

100-lead VFBGA, 7 x 7 mm, pitch 0.65 mm

Revision A - Industrial (-40° C to +85° C), Revision B -(-40° C to +105° C)

USB 2.0 Device: 12 Mbps, 2668 byte FIFO, up to 8 bidirectional Endpoints, on-chip transceiver

Up to two USARTs with ISO7816, IrDA®, RS-485, SPI, Manchester and Modem Mode

Two 2-wire UARTs

Up to two 2-Wire Interface modules (I2C-compatible), one SPI, one Serial Synchronous Controller (I2S), one high-speed Multimedia Card Interface (SDIO/SD Card/MMC)

Two 3-channel 16-bit Timer Counters with capture, waveform, compare and PWM mode, Quadrature decoder logic and 2-bit Gray up/down counter for stepper motor

4-channel 16-bit PWM with complementary output, fault input, 12-bit dead time generator counter for motor control

32-bit Real-time Timer and RTC with calendar, alarm and 32 kHz trimming features

256-bit General Purpose Backup Registers (GPBR)

32-bit Cyclic Redundancy Check Calculation Unit (CRCCU) for data integrity check of off-/on-chip memories

79 I/O Lines with external interrupt capability (edge or level sensitivity), debouncing, glitch filtering and on-die series resistor termination

Three 32-bit Parallel Input/Output Controllers, Peripheral DMA-assisted Parallel Capture mode

16-channel, 1Msps ADC with differential input mode and programmable gain stage and auto calibration

One 2-channel 12-bit 1Msps DAC

One Analog Comparator with flexible input selection, selectable input hysteresis

Serial Wire/JTAG Debug Port(SWJ-DP)

Debug access to all memories and registers in the system, including Cortex-M4 register bank when the core is running, halted, or held in reset.

Serial Wire Debug Port (SW-DP) and Serial Wire JTAG Debug Port (SWJ-DP) debug access.

Flash Patch and Breakpoint (FPB) unit for implementing breakpoints and code patches.

Data Watchpoint and Trace (DWT) unit for implementing watchpoints, data tracing, and system profiling.

Instrumentation Trace Macrocell (ITM) for support of printf style debugging.

IEEE1149.1 JTAG Boundary-scan on all digital pins.

ASF-Atmel software Framework – SAM software development framework

Integrated in the Atmel Studio IDE with a graphical user interface or available as standalone for GCC, IAR compilers.

DMA support, Interrupt handlers Driver support

USB, TCP/IP, Wi-Fi and Bluetooth, Numerous USB classes, DHCP and Wi-Fi encryption Stacks

RTOS integration, FreeRTOS is a core component

Related Products

ATSAMA5D36A-CU

Microchip Technology, Inc

LFBGA-324

ATMEGA32M1-AU

Microchip Technology, Inc

TQFP-32

[ATXMEGA128D3-AU]

Microchip Technology, Inc

TQFP-64

[ATTINY2313V-10SU]

Microchip Technology, Inc

SOIC-20

[ATMEGA64M1-15AZ]

Microchip Technology, Inc

TQFP-32

[ATMEGA16L-8PU]

Microchip Technology, Inc

PDIP-40

[ATTINY48-MU]

Microchip Technology, Inc

VQFN-32

[ATTINY4-TSHR]

Microchip Technology, Inc

SOT-23-6