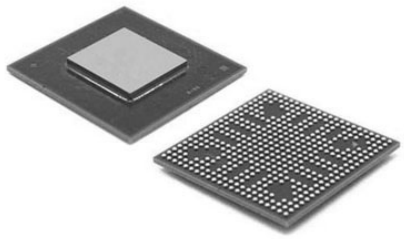
AD9650BCPZ-25

Data Sheet

Analog to Digital Converters - ADC 16Bit 25Msps Dual

Manufacturers	Analog Devices, Inc
Package/Case	LFCSP-64
Product Type	Data Conversion ICs
RoHS	Rohs
Lifecycle	



Images are for reference only

Please submit RFQ for AD9650BCPZ-25 or Email to us: sales@ovaga.com We will contact you in 12 hours. RFQ

General Description

The AD9650 is a dual, 16-bit, 25 MSPS/65 MSPS/80 MSPS/ 105 MSPS analog-to-digital converter (ADC) designed for digitizing high frequency, wide dynamic range signals with input frequencies of up to 300 MHz.

The dual ADC core features a multistage, differential pipelined architecture with integrated output error correction logic. Each ADC features wide bandwidth, differential sample-and-hold analog input amplifiers, and shared integrated voltage reference, which eases design considerations. A duty cycle stabilizer is provided to compensate for variations in the ADC clock duty cycle, allowing the converters to maintain excellent performance.

The ADC output data can be routed directly to the two external 16-bit output ports or multiplexed on a single 16-bit bus. These outputs can be set to either 1.8 V CMOS or LVDS.

Flexible power-down options allow significant power savings, when desired.

Programming for setup and control is accomplished using a 3-wire SPI-compatible serial interface.

The AD9650 is available in a 64-lead LFCSP and is specified over the industrial temperature range of −40°C to +85°C.

PRODUCT HIGHLIGHTS

APPLICATIONS

On-chip dither option for improved SFDR performance with low power analog input.

Proprietary differential input that maintains excellent SNR performance for input frequencies up to 300 MHz.

Operation from a single 1.8 V supply and a separate digital output driver supply accommodating 1.8 V CMOS or LVDS outputs.

Standard serial port interface (SPI) that supports various product features and functions, such as data formatting (offset binary, twos complement, or gray coding), enabling the clock DCS, power-down, and test modes.

Pin compatible with the AD9268 and other dual families, AD9269, AD9251, AD9231, and AD9204. This allows a simple migration across resolutions and bandwidth.

Features

1.8 V analog supply operation

1.8 V CMOS or LVDS output supply

SNR

82 dBFS at 30 MHz input and 105 MSPS data rate

83 dBFS at 9.7 MHz input and 25 MSPS data rate

SFDR

90 dBc at 30 MHz input and 105 MSPS data rate

95 dBc at 9.7 MHz input and 25 MSPS data rate

82 dBFS at 30 MHz input and 105 MSPS data rate

83 dBFS at 9.7 MHz input and 25 MSPS data rate

90 dBc at 30 MHz input and 105 MSPS data rate

95 dBc at 9.7 MHz input and 25 MSPS data rate

Low power

328 mW per channel at 105 MSPS

119 mW per channel at 25 MSPS

Integer 1-to-8 input clock divider

See data sheet for additional features

328 mW per channel at 105 MSPS

119 mW per channel at 25 MSPS

Download AD9650-EP data sheet (pdf)

Application

Industrial instrumentation

X-Ray, MRI, and ultrasound equipment

High speed pulse acquisition

Chemical and spectrum analysis

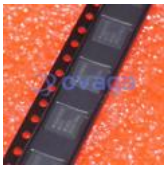
Direct conversion receivers

Multimode digital receivers

Smart antenna systems

General-purpose software radios

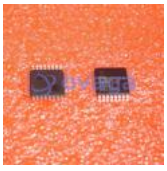
Related Products



ADAS3022BCPZ

Analog Devices, Inc

LFCSP-40



AD7266BSUZ

Analog Devices, Inc

TQPF-32

AD574AJNZ

Analog Devices, Inc

PDIP-28

AD7401YRWZ

Analog Devices, Inc

SOIC-16

AD7938BSUZ

Analog Devices, Inc

TQFP-32

AD7192BRUZ-REEL

Analog Devices, Inc

TSSOP-24

AD7124-8BCPZ-RL7

Analog Devices, Inc

LFCSP-32

AD9680BCPZ-500

Analog Devices, Inc

LFCSP-64