ATSAMS70J19A-AN

Data Sheet

ARM MCU, SAM S70 Series, SAM32 Family SAM S Series Microcontrollers, ARM Cortex-M7, 32bit, 300 MHz

Manufacturers	Microchip Technology, Inc
Package/Case	LQFP-64
Product Type	Embedded Processors & Controllers
RoHS	Green
Lifecycle	

Images are for reference only

Please submit RFQ for ATSAMS70J19A-AN or Email to us: sales@ovaga.com We will contact you in 12 hours. RFQ

General Description

The Microchip SAMS70J19 devices are members of a flash microcontrollers family based on the high-performance 32-bit ARM Cortex-M7 processor with Floating Point Unit (FPU). These devices operate at up to 300MHz and feature up to 2048 Kbytes of Flash, up to 384 Kbytes of multi-port SRAM and configurable Instruction and Data Tightly Couple Memories to leverage the advanced DSP capabilities of the core. SAMS70J19 features multiple communication interfaces including a HS USB Host and Device, a HS SDCard/SDIO/MMC interface, USARTs, SPIs and multiple TWIs. Analog features include dual 2Msps 12-bit ADCs with analog front end offering offset and gain error correction, and 2Msps 12-bit DAC.

The SAMS70J19 is available in 64-pin QFP and QFN package options.

Supported by MPLAB X IDE and MPLAB Harmony.

Features

S70 Features

Core

ARM Cortex-M7 running at up to 300 MHz(1)

16 Kbytes of ICache and 16 Kbytes of DCache with Error Code Correction (ECC)

Simple- and double-precision HW Floating Point Unit (FPU)

Memory Protection Unit (MPU) with 16 zones

DSP Instructions, Thumb®-2 Instruction Set

Embedded Trace Module (ETM) with instruction trace stream, including Trace Port Interface Unit (TPIU)

Memories

Up to 2048 Kbytes embedded Flash with unique identifier and user signature for user-defined data

Up to 384 Kbytes embedded Multi-port SRAM

Tightly Coupled Memory (TCM) interface with four configurations (disabled, 2 x 32 Kbytes, 2 x 64 Kbytes, 2 x 128 Kbytes)

16 Kbytes ROM with embedded Boot Loader routines (UART0, USB) and IAP routines

16-bit Static Memory Controller (SMC) with support for SRAM, PSRAM, LCD module, NOR and NAND Flash with on-the-fly scrambling

16-bit SDRAM Controller (SDRAMC) interfacing up to 256 MB and with on-the-fly scrambling

System

Embedded voltage regulator for single-supply operation

Power-on-Reset (POR), Brown-out Detector (BOD) and Dual Watchdog for safe operation

Quartz or ceramic resonator oscillators: 3 to 20 MHz main oscillator with failure detection, 12 MHz or 16 MHz needed for USB operations. Optional low-power 32.768 kHz for RTC or device clock

RTC with Gregorian calendar mode, waveform generation in low-power modes

RTC counter calibration circuitry compensates for 32.768 kHz crystal frequency variations

32-bit low-power Real-time Timer (RTT)

High-precision 4/8/12 MHz internal RC oscillator with 4 MHz default frequency for device startup. In-application trimming access for frequency adjustment. 8/12 MHz are factory-trimmed.

32.768 kHz crystal oscillator or embedded 32 kHz (typical) RC oscillator as source of low-power mode device clock (SLCK)

One 500 MHz PLL for system clock, one 480 MHz PLL for USB high-speed operations

Temperature Sensor

One dual-port 24-channel central DMA Controller (XDMAC)

Low-Power Features

Low-power Sleep, Wait and Backup modes, with typical power consumption down to 1.1 µA in Backup mode with RTC, RTT and wake-up logic enabled

Ultra-low-power RTC and RTT

1 Kbyte of backup RAM (BRAM) with dedicated regulator

Peripherals

USB 2.0 Device/Mini Host High-speed (USBHS) at 480 Mbps, 4-Kbyte FIFO, up to 10 bidirectional endpoints, dedicated DMA

12-bit ITU-R BT. 601/656 Image Sensor Interface (ISI)

Three USARTs. USART0/1/2 support LIN mode, ISO7816, IrDA®, RS-485, SPI, Manchester and Modem modes; USART1 supports LON mode.

Five 2-wire UARTs with SleepWalking support

Three Two-Wire Interfaces (TWIHS) (I2 C-compatible) with SleepWalking support

Quad I/O Serial Peripheral Interface (QSPI) interfacing up to 256 MB Flash and with eXecute-In-Place and onthe-fly scrambling

Two Serial Peripheral Interfaces (SPI)

One Serial Synchronous Controller (SSC) with I2S and TDM support

Two Inter-IC Sound Controllers (I2SC)

One High-speed Multimedia Card Interface (HSMCI) (SDIO/SD Card/e.MMC)

Four Three-Channel 16-bit Timer/Counters (TC) with Capture, Waveform, Compare and PWM modes, constant on time. Quadrature decoder logic and 2-bit Gray Up/Down Counter for stepper motor

Two 4-channel 16-bit PWMs with complementary outputs, Dead Time Generator and eight fault inputs per PWM for motor control, two external triggers to manage power factor correction (PFC), DC-DC and lighting control.

Two Analog Front-End Controllers (AFEC), each supporting up to 12 channels with differential input mode and programmable gain stage, allowing dual sample-and-hold at up to 2 Msps. Gain and offset error autotest feature.

One 2-channel 12-bit 1Msps-per-channel Digital-to-Analog Controller (DAC) with differential and oversampling modes

One Analog Comparator (ACC) with flexible input selection, selectable input hysteresis

Cryptography

True Random Number Generator (TRNG)

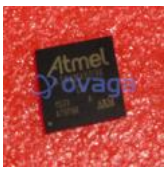
AES: 256-, 192-, 128-bit Key Algorithm, Compliant with FIPS PUB-197 Specifications−Integrity Check Monitor (ICM). Supports Secure Hash Algorithm SHA1, SHA224 and SHA256.

I/O

Up to 114 I/O lines with external interrupt capability (edge- or level-sensitivity), debouncing, glitch filtering and On-die Series Resistor Termination

Five Parallel Input/Output Controllers (PIO)SAMD10, 8KB Flash, 4KB RAM, low ocst, ARM Cortex M0+, low power, 14-pin

Related Products



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