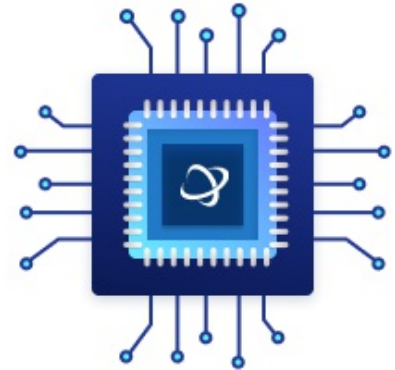


2-Output 3.3V PCIe Gen1–5 Clock Fanout Buffer with LOS

Manufacturers	Renesas Technology Corp
Package/Case	
Product Type	Clock & Timer ICs
RoHS	
Lifecycle	



Images are for reference only

Please submit RFQ for 9DBL0255NLGI8 or [Email to us: sales@ovaga.com](mailto:sales@ovaga.com) We will contact you in 12 hours.

[RFQ](#)

General Description

The device is a 2-output PCIe clock fanout buffers for PCIe Gen1–5 applications. It has an open drain Loss of Signal (LOS) output to indicate the absence or presence of an input clock.

For information regarding evaluation boards and material, please contact your local sales representative.

Features

Integrated terminations

85Ω transmission lines require 0 termination resistors

100Ω transmission lines require only 2 series resistors per output

OE pin for each output supports CLKREQ# applications

Intelligent power-down mode when all OE# pins are high (all outputs off)

Spread-spectrum tolerant

Open drain LOS# output indicates a loss of the input clock and returns the outputs to a Low/Low state

Flexible power sequencing: Input clock is internally biased so a floating input clock will not inject noise into system

Power Down Tolerant: Control inputs will not clamp to ground or VDD if a signal is applied before chip VDD is applied

Space saving 3 × 3 mm 16-VFQFPN

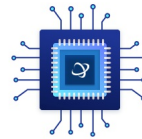
Easy AC-coupling to other logic families; see application note AN-891.

Related Products



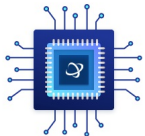
[9DB106BFILF](#)

Renesas Technology Corp
28-SSOP (0.209, 5.30mm Width)



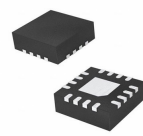
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Renesas Technology Corp



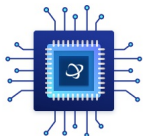
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Renesas Technology Corp



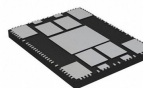
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Renesas Technology Corp
24-VFQFN



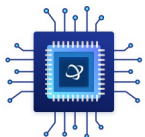
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Renesas Technology Corp



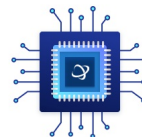
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Renesas Technology Corp
VFQFPN-40



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[9DBL0442BKILF](#)

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