

2.5V to 5.5V, 115 μ A Parallel Interface Single Voltage Output 12-Bit DAC; Package: TSSOP; No of Pins: 20; Temperature Range: Industrial

Manufacturers	Analog Devices, Inc
Package/Case	TSSOP-20
Product Type	Data Conversion ICs
RoHS	Rohs
Lifecycle	



Images are for reference only

Please submit RFQ for AD5341BRUZ or [Email to us: sales@ovaga.com](mailto:sales@ovaga.com) We will contact you in 12 hours.

[RFQ](#)

General Description

The AD5330/AD5331/AD5340/AD5341 have a parallel interface. CS selects the device and data is loaded into the input registers on the rising edge of WR.

The GAIN pin allows the output range to be set at 0 V to VREF or 0 V to $2 \times VREF$.

Input data to the DACs is double-buffered, allowing simultaneous update of multiple DACs in a system using the LDAC pin.

An asynchronous CLR input is also provided, which resets the contents of the input register and the DAC register to all zeros. These devices also incorporate a power-on reset circuit that ensures that the DAC output powers on to 0 V and remains there until valid data is written to the device.

The AD5330/AD5331/AD5340/AD5341 are available in thin shrink small outline packages (TSSOP).

Features

Single 12-Bit DAC in 20-Lead TSSOP

Low power operation: 115 μA @ 3 V, 140 μA @ 5 V

Power-down to 80 nA @ 3 V, 200 nA @ 5 V via PD Pin

2.5 V to 5.5 V power supply

Double-buffered input logic

Guaranteed monotonic by design over all codes

Buffered/unbuffered reference input options

See Data Sheet for Additional Information

Application

Portable battery-powered instruments

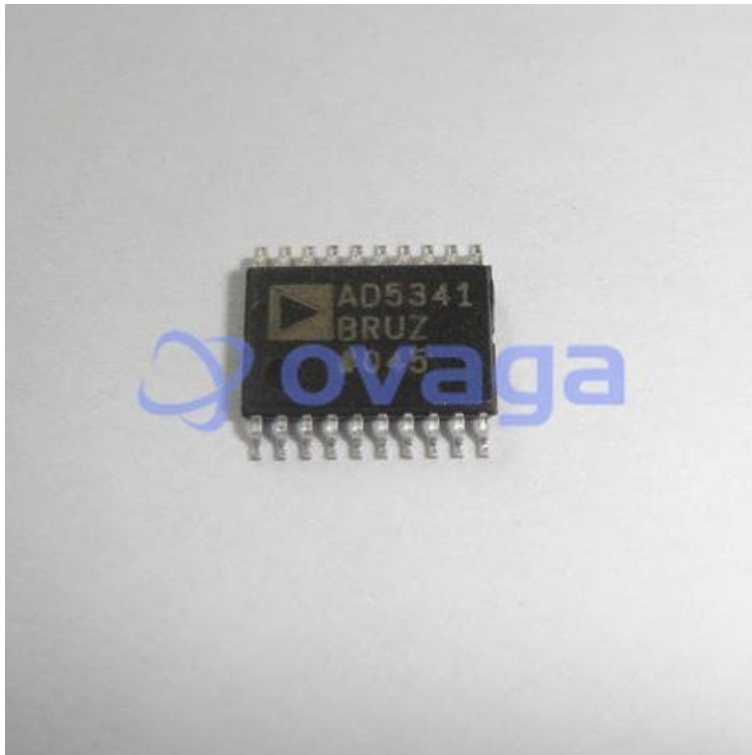
Digital gain and offset adjustment

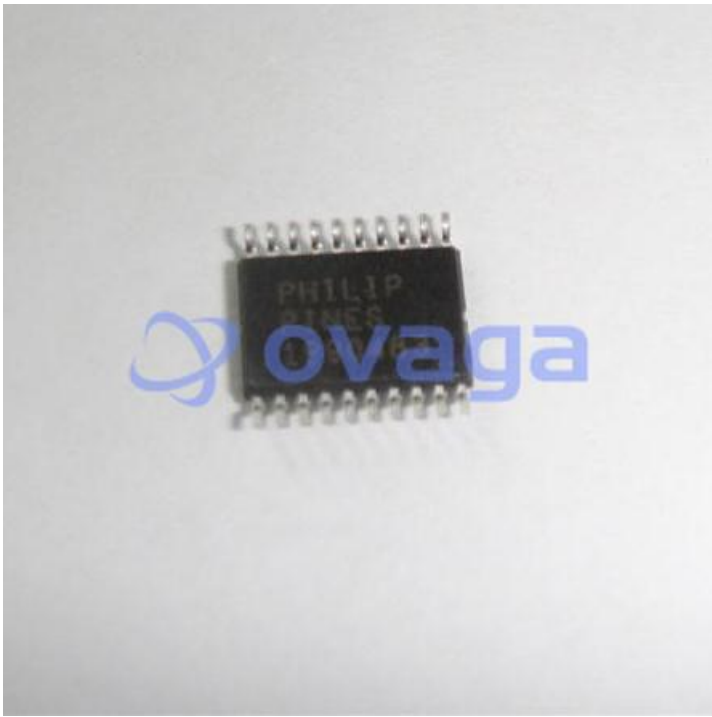
Programmable voltage and current sources

Programmable attenuators

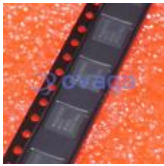
Industrial process control

Data Sheet, Rev. A, 2/08





Related Products



[ADAS3022BCPZ](#)

Analog Devices, Inc
LFCSP-40



[AD574AJNZ](#)

Analog Devices, Inc
PDIP-28



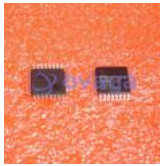
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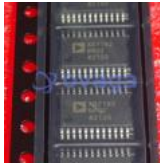
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[AD9680BCPZ-500](#)

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